PLL and Injection Locked PLL (ILPLL) Operations of a Push-Pull Self Oscillating Mixer (SOM)

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Abstract — **This paper presents the experimental results of a push-pull Self-Oscillating Mixer (SOM) tunable in a range of 421-463 MHz operating in PLL and Injection Locked PLL (ILPLL) regimes. By careful selection of the oscillator feedback resistor, an excellent down-conversion gain of up to 24.3 dB is observed. As a result, for the first time, the phase detection is performed as part of the SOM without the need for an external phase detector and gain stages. Issues such as tuning voltage-frequency variation, SOM phase-frequency variation, tracking range, pull in range, phase noise, and SOM phase controllability are discussed in the paper.**

I. INTRODUCTION

Self-oscillating mixer (SOM) circuits combine both local oscillators and mixer functions [1,2]. SOM with push-pull topology has been previously proposed for wireless communication applications in low power consuming front end circuits with –2 dB down-conversion gain [2] and a suhharmonically injected 12 GHz Injection Locked PLL (ILPLL) for phase and frequency locking as well as phase control of the output signal [3]. While the former application utilizes only open-loop Injection Locking (IL) [4], the latter needs an external phase detector for Phase Locked Loop (PLL) operation.

This paper presents for the first time the experimental results of closed-loop operation of SOM, where phase detection (mixing) function is performed by the SOM itself. The oscillator operates on a 3.3 V supply, covering a free running frequency of 421-463 MIIz. By careful selection of base resistor in push-pull transistor pair, a down-conversion mixing gain as high as 24.3 dB is measured, which is much higher than the one reported previously [2]. The need for gain stages in the loop filter is avoided by having such a high mixing gain. Both PLL and ILPLL operations are studied in terms of the phase relation between the locked oscillator output and the input injection (reference) signal and the variation of tuning voltage (built up through the closed-loop) with the injection frequency. The phase noise of the locked SOM is studied as well as the phase tuning range of ILPLL that is controlled by adjusting a reference DC signal introduced in the loop filter circuit.

II. CLOSED-LOOP SOM

Fig. 1.a illustrates the schematic of the SOM circuit. SOM is realized on Rogers 4003 60-mil-thick substrate. The design is based on a 3.3 V supply. Resonator consists of an abrupt varactor (C_{0V}/C_{3V} = 2, C_{0V} = 9.2 pF) and a 7.15 nH inductor (Q = 63 @ 500 MHz). BJT transistors have f_t = 12 GHz and β =110. Bias currents are 4.3 mA for Q_1 and Q_2 and 7.1 mA for Q_3, and a total power of 9.6 mW is consumed in SOM. The presence of an inductor (L_0) in collector bias of the transistors allows a swing of 2.3 V_{p-p} on the collector voltage.

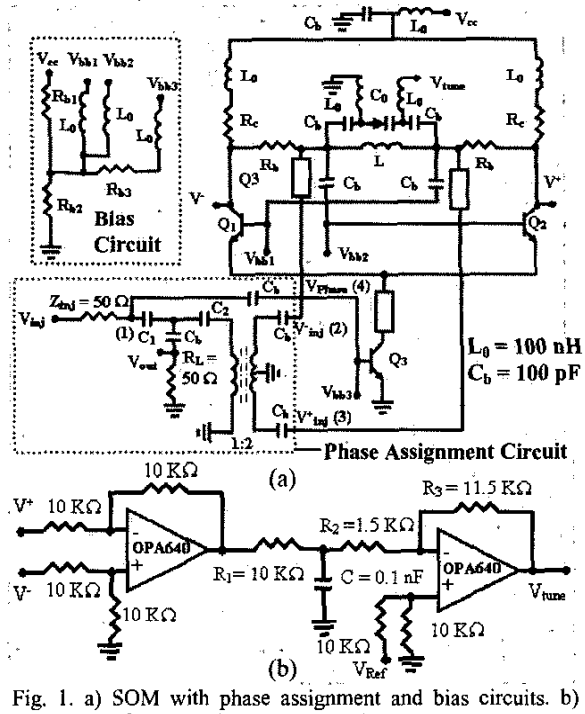

Fig. 1. a) SOM with phase assignment and bias circuits. b) Schematic of the loop filter; second order loop.

The phase assignment circuit (cf. Fig. 1.a) splits the signal from an injection (reference, 1) input (V_{inj}, Z_{inj} = 50 Ω) to V_{inj}^+ (3) and V_{inj}^- (2) signals (180° out of phase), and a signal 90° out of phase with them (V_{phase}, 4) as shown in Fig. 1.a. The design integrates the 50 Ω load as part of the phase assignment circuit. This avoids

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the need for an additional resistor, which dissipates a portion of the injection signal. For 50 Ω terminations, $|S_{21}|$ = -12 dB, and $|S_{41}|$ = -2 dB, where $\angle(S_{41}/S_{21}) = 90°$. The phase shift of 90° is necessary assuming a sinusoidal phase detection response. For this phase assignment circuit loaded by SOM, values of C_1 = 10 pF and C_2 = 10 pF are selected experimentally, close to their design values.

Fig. 1.b illustrates the schematic of the loop filter with one pole making the closed-loop of second order. Two opamps with measured unity gain bandwidth of 120 MHz are used to buffer the phase detected signal, level shift it, and apply it to the varactor. The filter transfer function is $H(f) = -G/(1+f/f_p)$, where $f_p = 1/2\pi(R_1\|R_2)C$ = 1.22 MHz and DC gain, $G = R_3/(R_1+R_2) = 1$. In addition, the varactor voltage V_{tune} (cf. Fig. 1.) has an adjustable DC level of V_{Ref}. With a non-zero C_1 the circuit of Fig. 1. can be identified as an ILPLL, whereas with $C_1 = 0$ (open circuit), the circuit can be regarded as a PLL.

III. PHASE DETECTION (MIXING)

The down-conversion mixing of SOM [2] is studied by opening the loop at V_{tune}, removing C_1, and setting the varactor voltage to zero. For V_{tune} = 0 V, P_{inj} = -30 dBm, and Δf (i.e., the frequency difference) = 10 MHz, simulations are performed to observe the change in conversion gain and output power of the SOM with R_b,. The results are presented in Table I. Below R_b = 0.1 KΩ, a spurious oscillation at 1.45 GHz dominates, while above R_b = 0.9 KΩ, the oscillation vanishes because of the decrease of the oscillator loop gain. As a compromise between gain and power, R_b = 0.24 KΩ is selected.

Table I. Simulation results of the change of conversion gain (CG) and output power (P_{out}) of the SOM with R_b (V_{tune} = 0 V, P_{inj} = -30 dBm, and Δf = 10 MHz).

R_b (KΩ)	0.1	0.17	0.24	0.5	0.75
CG (dB)	3.7	13.7	16.4	11	-9.8
P_{out} (dBm)	-3.2	-6.6	-10.5	-18.1	-28.0

The measured conversion gain for various Δf is also shown in Fig. 2 for P_{inj} = -20, -30, -40, -50 dBm and is compared with the simulation for P_{inj} = -30 dBm. At each power level, the mixed signal will not be obtained for a frequency difference lower than a certain limit, below which the injection locking through V_{phase} occurs. This limit is 3 MHz for P_{inj} = -30 dBm. Note that this is different from the main injection locking that would have been present with C_1 in place. The conversion gain is a strong function of frequency, due to the frequency response of the loop filter. Moreover, it is poor for P_{inj} = -20 dBm and increases with decreasing the power level. The deviation around 50 MHz from a monotonic decrease is due to transmission line effects in opamps connections, not accounted for in the simulation. For P_{inj} = -30 dBm, by considering the impact of loop filter response in measured results of Fig. 3, the DC conversion gain is estimated to be 25.8 dB that corresponds to a phase detection gain (sensitivity) of K_d = 0.19 V/Rad.

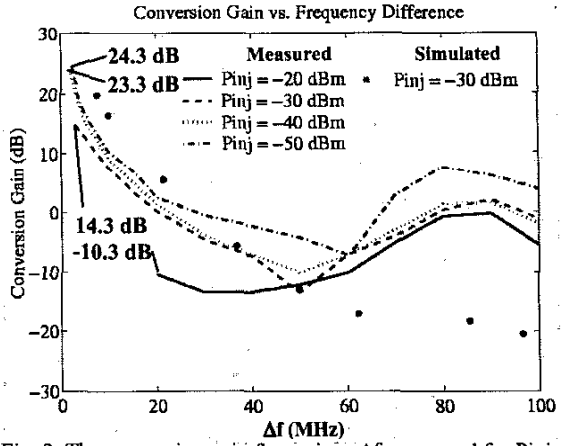

Fig. 2. The conversion gain for various Δf measured for Pinj = -20, -30, -40, -50 dBm and simulated for Pinj = -30 dBm.

IV. PLL AND ILPLL OPERATIONS

For ILPLL, the oscillation frequency and power level as a function of V_{Ref} are shown in Fig. 3 for P_{inj} = 0 W (i.e., no injection). To obtain the simulated free running oscillation as close as possible to the measured results, the distributed nature of the resonator should be modeled accurately. Furthermore, the capacitive nature of the phase assignment circuit has a significant impact on lowering both the oscillation frequency and tuning range. For this circuit, if all the capacitors are shorted, the simulation illustrates a much higher tuning range of 424 to 549 MHz. From Fig. 3, the measured power is –9.5 to –11.7 dBm with the second and third harmonics about 30 and 25 dB lower respectively. The results for PLL are quite similar. Oscillation gain (K_v) depends on V_{Ref}. For V_{Ref} = 0 and 0.5 V, K_v = 32 and 25.4 MHz/V respectively. It decreases with increasing the varactor bias. Assuming K_d = 0.19 V/Rad and $K_v = (2\pi)32$ MRad/V.S, the open- loop gain is K_vK_d = 39 MRad/S that corresponds to f_n = 2.7 MHz, ζ = 0.22 [5].

In order to study the closed-loop, Fig. 4 illustrates the observed change of the DVM reading of varactor tuning voltage, built up through the loop, as a function of frequency, for P_{inj} = -30 dBm. The results for PLL with V_{Ref} = 0 V and ILPLL with V_{Ref} = 0 and 0.5 V are shown. A phase variation with the frequency is also studied, where the injection input is taken from port #1 of a network analyzer and the oscillator output is connected to port #2. Fig. 5 illustrates S_{21} for the three

cases. The network analyzer's source power is set at -2 dBm, and a 28 dB attenuator is externally added at port #1 to make a -30 dBm injection. Note that the frequency range swept on the network analyzer corresponds to the solid line (increasing frequency) in Fig. 4 as the frequency sweep is from left to right in Fig. 5. Moreover, the corresponding frequency ranges shown in Figs. 4 and 5 are slightly different, due to the loading from DVM, monitoring the voltage in Fig. 4. Also, note that the injection has caused a decrease in free running frequency, approximated as the midpoint of the tracking range in Fig. 4, compared to the free running SOM of Fig. 3.

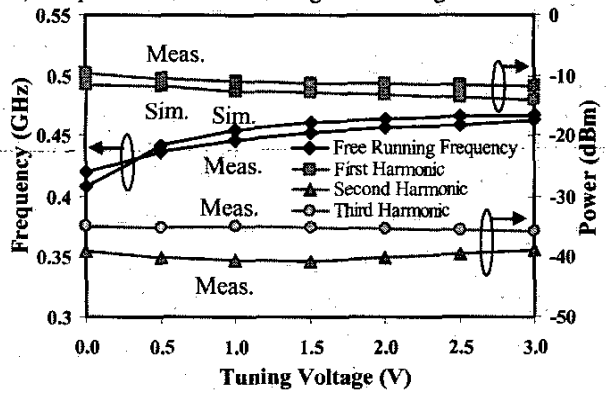

Fig. 3. Measurement (Meas.) and/or simulation (Sim.) results of closed-loop free running frequency, and the power of the first three harmonics, for V_{out}, as a function of V_{Ref} (P_{inj} = 0 W).

For PLL, the so-called pull in range, a range within which the lock can be acquired, is within the tracking (hold in) range [5]. For ILPLL and V_{Ref} = 0 V, while at the lower frequencies within the pull in range no difference in behavior exists between the increasing and decreasing the frequency, the upper frequency portion shows a complex behavior (cf. Fig. 4). Within the pull in range, hystersis is observed from 403 to 410 MHz, in which V_{tune} experiences more negative values with decreasing frequency. Moreover, above 411 MHz, the PLL operation seems to be the only locking mechanism. This coincides with an abrupt 140° decline of the phase of Fig. 5.b at 413 MHz (Note that there is a difference between the ranges of the two figures due to DVM loading in Fig. 4.).

A particular feature of PLL is an abrupt change in the magnitude and phase of S_{21} of Fig. 5.a in the edges. When the oscillator breaks the lock, the free running oscillation continues to exist and is going to mix with the injection signal. On the other hand, ILPLL demonstrates a gradual reduction of the amplitude after the lock is broken (cf. Figs. 5.b and 5.c), where the output spectrum on the spectrum analyzer resembles that of a one-sided injection locking oscillation spectrum.

For ILPLL and V_{Ref} = 0.5 V, no difference between the tracking and pull in range exists. Furthermore, no tuning voltage hystersis or phase jump is observed. In fact, this is the case for V_{Ref} > 0.2 V. For PLL, what is observed in Fig. 4 is a typical voltage-frequency response, where by increasing the frequency the varactor voltage has to increase. In contrast, this figure proves that the situation is opposite in the case of ILPLL in here. It has to be emphasized that for both PLL and ILPLL the loop demonstrates instability with increasing the gain of the opamps or selecting inappropriate loop filter parameters.

For V_{tune} = 0.5 V and P_{inj} = -30 dBm, phase noise for ILPLL, IL, and PLL regimes is measured at the midpoint of the range and at the lower corner of the range 1 MHz before the lock is broken. At the midpoint, the phase noise is practically the same as the reference signal (-113 dBc/Hz @ 30 KHz). For the corner, the phase noise is degraded. At 30 KHz from the carrier, the phase noise degradation is 10, 14, and 6.5 dB for ILPLL, IL, and PLL respectively. Note that IL is the injection locked SOM, for which the loop is open at V_{tune} (cf. Fig. 1).

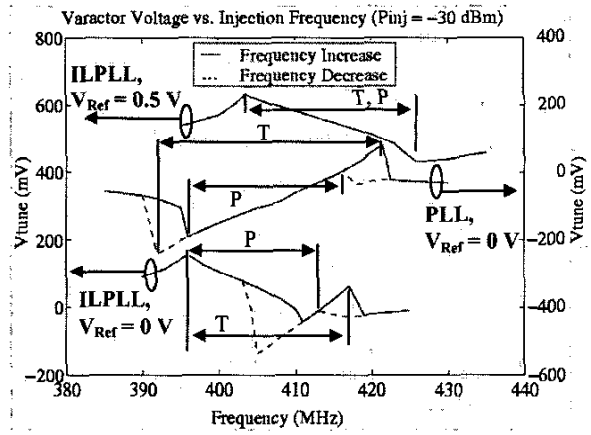

Fig. 4. Varactor tuning voltage versus frequency. Pull in (P) and tracking (T) ranges are identified. The results for both frequency increase (—) and decrease (...) are shown.

In a similar fashion suggested before [3], the phase of SOM can be controlled by changing V_{Ref}. For ILPLL, Fig. 6 illustrates the change of phase with V_{Ref}, for the center frequency of the pull in range in Fig. 4 for V_{Ref} = 0 V ($\Delta f/B$ = 0, with Δf being the frequency deviation from the center and B being the pull in range) and an off center higher frequency of $\Delta f/B$ = 0.4. Note that the latter provides a higher phase tuning range of 50.6° as V_{Ref} changes from 0 to 3 V, whereas in the former case, the lock is broken at about V_{Ref} = 0.8 V. The reason for such

observation is that with increasing V_{Ref}, the lower corner of the pull in range approaches the reference frequency. When $V_{Ref} = 0$, choosing this frequency closer to the upper edge of the pull in range guarantees that the lock would be maintained within a higher range of variation of V_{Ref}.

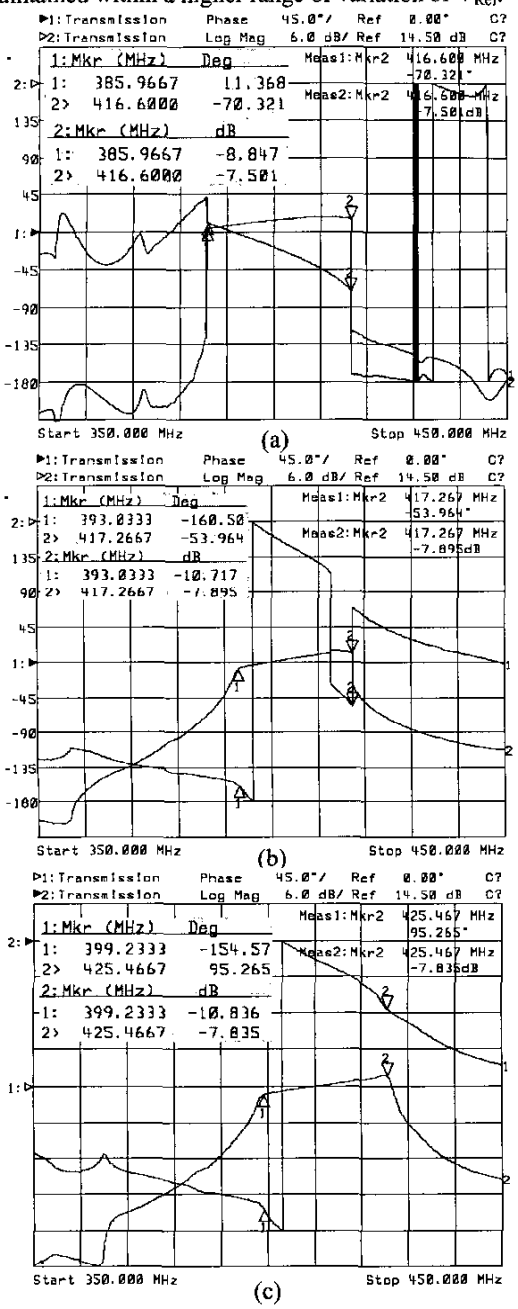

Fig. 5. Demonstration of $|S_{21}|$ and phase relationship ($\angle S_{21}$) between the injection and output signals for P_{inj} = -30 dBm; a) PLL and $V_{Ref} = 0$ V, b) ILPLL and $V_{Ref} = 0$ V, and c) ILPLL and $V_{Ref} = 0.5$ V.

V. CONCLUSIONS

PLL and ILPLL operations of an SOM circuit have been demonstrated. By careful design of SOM feedback, phase detection gain necessary for the closed-loop operation can be obtained solely by the SOM itself. External opamps are used for differential to single ended transformation and tuning voltage level adjustment. However, their presence is not a requirement for closed-loop operation, and a fully passive loop filter is possible. The tracking ranges of 7.8% and 5.9 % were observed for PLL and ILPLL respectively. Nonetheless, the observed variations of the varactor voltage built up by the loop are quite different between the two cases. SOM exhibits some sensitivity to loading from the injection locking inputs and stages that follow SOM (e.g., load). Simulations show that this can be remedied by introducing emitter follower transistors in the feedback path of SOM. An integrated version of such a circuit is currently being realized, where the oscillation frequency and phase of a 10 Gbps and higher clock recovery circuits are stabilized by ILPLL.

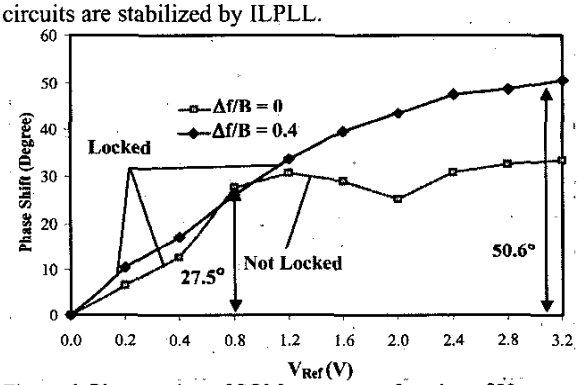

Figure 6. Phase tuning of SOM output as a function of V_{Ref}.

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